REMARKS

Examiner has rejected claims 1 through 3, 5 through 18 and 21 through 30 under 35 U.S.C. § 102(e) as being anticipated by USPN 5,978,578 (Azarya). Examiner has rejected claims 4, 16 through 18 and 31 through 41 under 35 U.S.C. § 103(a) as being unpatentable over Azarya in view of USPN 5,903,737 (Han). Examiner has rejected claims 19 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Azarya. Applicant has amended the claims to further clarify the subject matter Applicant views as the invention. Applicant respectfully traverses the rejection as to the claims as amended.

Azarya discloses an openbus system for control automation networks. Han discloses an apparatus and method for serial data communication utilizing general microcomputer.

The references, whether considered alone or in combination, do not disclose or suggest the subject matter set out in the claims of the present application.

For example, independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access controller, a host interface and an embedded processor. This functionality is not disclosed or suggested by the cited art.

Examiner has asserted that all the elements of claim 1 are found within Azarya at Figure 4, at column 9, lines 41 through 52, at column 20 (10?), lines 44 through 57 and at column 11, lines 6 through 38. However, these portions of Azarya do not disclose or suggest a chip that includes a media access controller, a host interface and an embedded processor.

For example, Figure 4 of Azarya discloses an openbus node controller 10 that includes interface circuitry boards 20, an embedded processor 22 and a network interface card 24 all connected to a bus. The openbus node controller 10 does not disclose or suggest the present invention. Specifically, claim 1 of the present Application sets out that a media access controller, a host interface and an embedded processor are all included *within a single chip*. However, the functionality within openbus node controller 10 is implemented within *boards* and *cards*. Presumably, each board or card includes several chips.

Azarya does not disclose a single chip that includes a media access controller, a host interface and an embedded processor. In fact, it is not clear which if any of the boards or cards within openbus node controller 10 implement a media access controller or a host interface.

Since Azarya does not disclose or suggest a single chip that includes a media access controller, a host interface and an embedded processor, Applicant respectfully traverses the rejection under 35 U.S.C. § 102(e) and respectfully requests reconsideration.

Similarly, independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and an embedded processor. This functionality is not disclosed or suggested by the cited art.

As discussed above, Azarya does not disclose a single chip that includes a media access controller, a host interface and an embedded processor. In fact, it is not clear which if any of the boards or cards within openbus node controller 10 implement a media access controller or a host interface. Since Azarya does not disclose or suggest a single chip

that includes a media access controller, a host interface and an embedded processor, Applicant respectfully traverses the rejection under 35 U.S.C. § 102(e) and respectfully requests reconsideration.

Likewise, claim 23 sets out a system. The system includes a network device. The network device includes a chip. The chip includes a media access controller and an embedded processor programmed to function as an HTTP manageability web server. This functionality is not disclosed or suggested by the cited art.

As discussed above, Azarya does not disclose a single chip that includes a media access controller and an embedded processor. In fact, it is not clear which if any of the boards or cards within openbus node controller 10 implement a media access controller. Since Azarya does not disclose or suggest a single chip that includes a media access controller and an embedded processor, Applicant respectfully traverses the rejection under 35 U.S.C. § 102(e) and respectfully requests reconsideration.

Also, independent claim 31 sets out a method of managing a network device including a host processor, an I^2C bus, and an I^2C-compliant device. In a first step of claim 31, a media access controller is used to receive network manageability information requests from a computer network. The media access controller communicates with the computer network independent of the host processor and the I^2C-compliant device. This is not disclosed or suggested by Azarya or Han. Particularly, neither Azarya or Han disclose or suggest using a *media access controller* to receive *network manageability information requests* from a computer network.

In a second step of claim 31, the I^2C bus is used to obtain network manageability information about the I^2C-compliant device. This is not disclosed or suggested by Azarya or Han. Particularly, neither Azarya or Han disclose or suggest using a I^2C bus to obtain network manageability information about a I^2C-compliant device.

In a third step, of claim 31, the media access controller is used to place the manageability information on the computer network. This is not disclosed or suggested by Azarya or Han. Particularly, neither Azarya or Han disclose or suggest using a media access controller to place manageability information on a computer network.

Since none of the steps of claim 31 are disclosed or suggested by Azarya or Han, whether considered alone or in combination, Applicant respectfully traverses the rejection under 35 U.S.C. § 103(a) and respectfully requests reconsideration.

Applicant notes that implementation of a web server chip, as set out in the claims of the present case, allows for implementation of network management at significantly reduced costs than is provided by prior art systems. Applicant believes that this invention is a significant, non-obvious improvement over prior art systems.

Applicant believes that this Amendment has placed the present case in condition for allowance and favorable action is respectfully requested.

Respectfully submitted,
DAVE GOH, ET AL.

By _____
Douglas L. Weller
Reg. No. 30,506

November 2, 2000
Santa Clara, California
(408) 985-0642